REMARKS

This amendment responds to the office action mailed May 22, 2003. In the office action the Examiner:

- allowed claims 1-7 and 20;
- rejected claims 8, 10-12, 15, 18, 19, 21-29, 37-45, 49-51, 55-58, 64, 65, 69, and 70-72 under 35 U.S.C. 102(e) as being anticipated by Woeste et al. (U.S. Patent No. 6,232,806);
- rejected claims 35, 36, 47, 48, 52-54, 59, 66-68 and 73 under 35 U.S.C. 103(a) as being unpatentable over Woeste et al. (U.S. Patent No. 6,232,806) as applied to claim 21; and
- objected to claims 9, 13, 14, 16, 17, 30-34, 46 and 60-63 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-7 and 20 have been allowed by the Examiner. Claim 8 has been canceled by the Applicant. After entry of this amendment, the pending claims are: claims 1-7 and 9-73.

Changes to the specification are grammatical only

The amendment in the paragraph at page 4 line 28 is required because it referred to master 24, when it should have referred to master 22. No new subject matter was added.

Claims 9, 31-34 and 60-63 should be allowed

The Examiner indicated claims 9, 31-34 and 60-63 are objected to as being dependent upon rejected base claims, but would be allowed if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In this amendment, claims 9, 31 and 60 have been rewritten in independent form including all of the limitations of the corresponding base claims 8, 21, and 50 respectively. Meanwhile, claims 32-34 and 61-63 are dependent upon claims 31 and 60 respectively. Therefore, claims 9, 31-34 and 60-63 should be allowed.

Claims 11-14, 15-19

Woeste et al. does not identify a selected phase delay associated with a selected slave device

Woeste et al. only teaches a method of indiscriminately distributing a clock signal

from a master device to a number of slave devices such that all the slave devices operate in a synchronous manner. As shown in Fig. 1A of Woeste et al., the method uses a plurality of phase detectors 54 and 64 in a master module 22 to estimate a plurality of phase differences between a reference clock signal provided by a primary slave module 24 and a plurality of feedback clock signals provided by a plurality of secondary slave modules 34 and 44.

After that, instead of selecting one phase difference from the plurality of phase differences, phase detectors 54 and 64 pass all the phase differences to a plurality of control logics 56 and 66 simultaneously. Each phase difference is applied by a control logic 56 or 66 to a respective variable delay line 52 or 62. Therefore, Woeste et al. does not disclose the step of selecting a particular phase delay in association with a particular slave.

In contrast, claim 11 and its dependent claims 12-14 of the present invention are directed to a method of operating a synchronized communication between a master device and a plurality of slave devices. The first step of the method is to assess a plurality of phase delays between the master device and the plurality of slave devices using a universal phase aligner associated with the master device. The second step is to select one phase delay from the plurality of phase delays and one slave device in association with the selected phase delay. The final step of the method is to communicate data between the master device and the selected slave device in accordance with the selected phase delay.

Similar to claim 11, claim 15 and its dependent claims 16-19 recite a master/slave system comprising a master device that utilizes a selected phase value from a plurality of phase values so as to establish synchronous communication between the master device and a selected slave device.

Therefore, neither claims 11-14 nor claims 15-19 are anticipated by Woeste et al..

Claims 15-19, 21-30, 35-36, 37-49, 50-59, 64-73

Woeste et al. teaches a simultaneous, not sequential, synchronization between a master device and a plurality of slave devices and Woeste et al. does not disclose an addressable phase value register bank or anything similar

Woeste et al. discloses a method of simultaneously adjusting the phases of a plurality of clock signals such that all secondary slave modules that receive the phase-adjusted clock signals operate in a synchronous manner. As shown in Fig. 1A of Woeste et al., this phase adjustment happens simultaneously for each variable delay line 52 or 62. Each phase detector estimates and stores only one phase difference, and different phase detectors

associated with different variable delay lines all operate in parallel with each other.

After receiving a phase difference from its corresponding phase detector, each control logic also applies the phase difference to a variable delay line in parallel to other control logics. As a result, the outputs of all the variable delay lines are always substantially in synch with the reference clock signal and thereby with each other.

In other words, the synchronization between a master module and a plurality of slave modules taught by Woeste et al. can be divided into multiple sub-synchronizations, one sub-synchronization for each slave module. All the sub-synchronizations occur at the same time.

Even though the synchronization in the present invention can also be divided into multiple sub-synchronizations, these sub-synchronizations do not happen at the same time. As shown in Figs. 3 and 5 of the present invention, a plurality of phase values are estimated by the master device sequentially, not simultaneously, and at the end of a sub-synchronization for one slave device, the master device identifies a phase value for this slave device.

Furthermore, unlike Woeste et al. in which the plurality of phase differences between the plurality of slave devices and the master device are stored in a plurality of phase detectors and control logics, the plurality of phase values in the present invention are stored in a single device, an addressable phase value register bank 74, as shown in Fig. 2.

Claim 15 and its dependent claims 16-19 recite an addressable phase value register bank in a master device that stores a plurality of phase values for a plurality of slave devices. After storing a phase value at a unique address in the addressable phase value register bank, the master device does not need to keep in synch with the slave device any longer. The master device re-synchronizes with the slave device only when it decides to communicate with it.

However, in order to re-synchronize with the slave device, the master and slave devices do not need to go through the same synchronization process one more time as Woeste et al. does. Instead, the master device simply retrieves the phase value associated with the slave device from the addressable phase value register bank and uses it to alter its system clock signal accordingly so that the master device and the slave device operate in a synchronous manner. If the master device later chooses to communicate with another slave device, it will retrieve another phase value from the register bank and act in a similar way.

Similarly, claim 21 and its dependent claims 22-30 and 35-36 recite a method of calibrating data transmission from a master device to a slave device over a data line. The

method first determines a phase offset value between the master device and the slave device over the data line and then stores the phase offset value in an addressable register bank. Later on, when the master device decides to transmit data to the slave device over the data line, it does not need to re-estimate the phase offset value as Woeste et al. does, but simply retrieves the corresponding phase offset value from the register bank and uses it to alter its system clock signal so as to establish a synchronous data transmission from the master device to the slave device.

Claim 37 and its dependent claims 38-49 recite a method of calibrating control information transmission from a master device to a slave device over a request line. Similar to claim 21 and its dependent claims, the method stores a phase offset value between the master device and the slave device over the request line in an addressable register bank and retrieves it from the register bank when the master device needs to establish a synchronous control information transmission to the slave device over the request line.

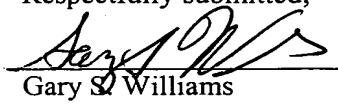
Claim 50 and its dependent claims 51-59 recite a master device that implements the method recited in claim 21 and its dependent claims, and claim 64 and its dependent claims 65-73 recites a master device that implements the method recited in claim 37 and its dependent claims.

Therefore, claim 15 and its dependent claims 16-19, claim 21 and its dependent claims 22-30 and 35-36, claim 37 and its dependent claims 38-49, claim 50 and its dependent claims 51-59, and claim 64 and its dependent claims 65-73 are not anticipated by and patentable over Woeste et al.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 493-4935, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: August 22, 2003



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